


UART interface layout	
Pin No.	Signal
1	+5V
2	+3.3V (output)
3	GND
4	RX
5	TX

Dept.	Technical reference	Created by FiSens	13.07.2021	Approved by	
		Document type	Document status		
		Title FiSpec FBG X100	DWG No.		
		Rev. 04	Date of issue 2021-07-13	Sheet 1/1	